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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/783,474	02/20/2004	Jian-Shen Yu	B-5381 621721-5	7461

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EXAMINER	
SHERMAN, STEPHEN G	
ART UNIT	PAPER NUMBER
2629	
MAIL DATE	DELIVERY MODE
07/25/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/783,474	YU ET AL.	
	Examiner	Art Unit	
	Stephen G. Sherman	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 June 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *4 and 8* is/are allowed.

6)☒ Claim(s) *2 and 6* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to the amendment filed 18 June 2007. Claims 2, 4, 6 and 8 are pending. Claims 1, 3, 5,and 7 have been cancelled.

Response to Arguments

2. Applicant's arguments filed 18 June 2007 with respect to clams 2 and 4 have been fully considered but they are not persuasive.

On page 7 of the applicant's response the applicant argues that Higashi does not teach, disclose or suggest a capacitor whose value determines a feed-through voltage drop of the first TFT. The applicant argues on page 7, lines 6-15 that the capacitance shown in Higashi is the capacitance of the data line itself, and that the value of the data line capacitance can not be easily changed for counteracting the feed-through voltage drop caused by a parasitic capacitor of the MOS transistor. The applicant then argues on page 7, lines 16-22 of the response, that according to line 18, page 8 to line 2, page 9 of the present application, a formula of the feed-through voltage drop is presented showing that the feed-through voltage drop is changed as a function of the capacitance of the counteracting device. Then on page 8, lines 2-3 of the response the applicant states: "The value of such a capacitor related to the feed-through voltage drop is not disclosed in Higashi." The examiner respectfully disagrees.

The structure shown in Higashi is the same as that shown in the applicant's specification. Figure 25B of Higashi clearly shows an added capacitor that is not representative of the capacitance of the data line. There inherently is a parasitic capacitor across the transistor, and the connection of the "counteracting" capacitor and transistor shown in Figure 25B is the same as that of the applicant's. Therefore, the capacitor will inherently act to counteract the effect of the parasitic capacitor, i.e. reduce the feed-through voltage drop. Whether, in the reference, the capacitance of the capacitor is changed to determine the feed-through voltage drop or not doesn't matter because this feature is NOT claimed. The capacitor has a value and this value will

inherently determine the feed-through voltage drop and thus, Higashi anticipates the CLAIMED invention.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 2 and 4 are rejected under 35 U.S.C. 102(b) as being anticipated by Higashi (US 6,023,260).

Regarding claim 2, Higashi discloses a sampling circuit (Figure 3, circuit 261) for an analog signal according to a clock signal, comprising:

a first thin film transistor (TFT) (Figure 3, transistor 410),

having a first electrode to receive the analog signal (Figure 3 shows that transistor 410 receives on a first electrode analog signal S1 as explained in column 7, lines 7-10.),

a control electrode to receive the clock signal (Figure 3 shows that the control electrode of transistor 410 is connected to the clock signal output 240.) and

a second electrode for sampling the analog signal when the clock signal is at a first logic level (Figure 3 shows that transistor 410 has a second electrode for sampling the analog signal when the clock signal turns the transistor on/off.); and

a capacitor between the second electrode and a reference potential node (Column 7, lines 34-38 explain that analog structure shown in Figure 25B as the data line drivers. Figure 25B shows capacitor 420 which is coupled between the second electrode and ground.),

wherein a feed-through voltage drop caused by a parasitic capacitor between the second electrode and the control electrode of the first TFT is determined according to the value of the capacitor (There is inherently a parasitic capacitance between the second electrode and the control electrode of the first TFT and given that Higashi has the same structure and connections of the capacitors and TFTs, then the value of the capacitor will determine the feed-through voltage drop caused by the parasitic capacitance.); and

wherein when the clock signal is changed from the first logic level to a second logic level, the capacitor reduces the feed-through voltage drop (The examiner understands that since the structure of Higashi is the same as the structure in the specification, the circuit of Higashi will inherently reduce the feed-through voltage drop caused by a parasitic capacitance when the transistor 410 is turned on/off by the clock signal.).

Regarding claim 6, Higashi discloses a liquid crystal display (Figure 3), comprising:

a plurality of display units, arranged in array (Figures 1A and 1B and column 4, lines 47-64.);

a plurality of data lines disposed corresponding to each line of the display units, wherein each data line provides a video signal to the corresponding display unit (Figure 3 D(1)-D(k) and column 7, lines 7-10.); and

a data driving circuit (Figure 1A, item 200 and column 4, lines 65-67.), having at least one sampling circuit, sampling an image signal to be the video signal according to a clock signal (Figure 3, circuit 261), and the sampling circuit comprising:

a first thin film transistor (TFT) (Figure 3, transistor 410),

having a first electrode to receive the analog signal (Figure 3 shows that transistor 410 receives on a first electrode analog signal S1 as explained in column 7, lines 7-10.),

a control electrode to receive the clock signal (Figure 3 shows that the control electrode of transistor 410 is connected to the clock signal output 240.) and

a second electrode for sampling the analog signal when the clock signal is at a first logic level (Figure 3 shows that transistor 410 has a second electrode for sampling the analog signal when the clock signal turns the transistor on/off.); and

a capacitor between the second electrode and a reference potential node (Column 7, lines 34-38 explain that analog structure shown in Figure 25B as the data

line drivers. Figure 25B shows capacitor 420 which is coupled between the second electrode and ground.),

wherein a feed-through voltage drop caused by a parasitic capacitor between the second electrode and the control electrode of the first TFT is determined according to the value of the capacitor (There is inherently a parasitic capacitance between the second electrode and the control electrode of the first TFT and given that Higashi has the same structure and connections of the capacitors and TFTs, then the value of the capacitor will determine the feed-through voltage drop caused by the parasitic capacitance.); and

wherein when the clock signal is changed from the first logic level to a second logic level, the capacitor reduces the feed-through voltage drop (The examiner understands that since the structure of Higashi is the same as the structure in the specification, the circuit of Higashi will inherently reduce the feed-through voltage drop caused by a parasitic capacitance when the transistor 410 is turned on/off by the clock signal.).

Allowable Subject Matter

5. Claims 4 and 8 allowed.

6. The following is a statement of reasons for the indication of allowable subject matter:

The primary reason for indicating allowable subject matter is that both claims 4 and 8 recite the limitation: " wherein the capacitor comprises a second TFT having a gate terminal coupled to the output terminal of the inversion device and a source and drain terminal both coupled to the second electrode," which is not found singularly or in combination within the prior art.

The closest prior art reference is Higashi (US 6,023,260) which teaches an inversion device with a transistor between the second electrode and an output terminal of the inversion device, however, Higashi fails to teach that the both the source and drain are coupled to the second electrode.

Conclusion

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stephen G. Sherman whose telephone number is (571) 272-2941. The examiner can normally be reached on M-F, 8:00 a.m. - 4:30 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amr Awad can be reached on (571) 272-7764. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

SS

16 June 2007

AMR A. AWAD
SUPERVISORY PATENT EXAMINER